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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,517	06/19/2001	Eugene A. Fitzgerald	Amber.5994A	2548

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Patent Administrator  
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EXAMINER

DUONG, KHANH B

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/884,517

Applicant(s)

FITZGERALD ET AL.

Examiner

Khanh Duong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 April 2004.  
2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,6-12,15 and 20-27 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1,6-12,15 and 20-27 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/8/04.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### ***Response to Amendment***

This Office Action is in response to the amendment filed on April 7, 2004.

Accordingly, claims 4, 5, 18 and 19 were cancelled, and claims 1 and 15 were amended.

Currently, claims 1, 6-12, 15 and 20-27 remain pending in the application.

### ***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on March 8, 2004 is considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 1, 6-12, 15, 20, 21, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lustig (U.S. 5,998,807) in view of Chu et al. (U.S. 5,906,951) and Canaperi et al. (US 6,524,935).**

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Lustig ("Lustig") discloses a CMOS circuit (see Figs. 1-9 and corresponding description) comprising : a heterostructure including a Si substrate 1, a relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer 4 on the Si substrate 1, and a strained channel layer 5 on the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer 4; the heterostructure further including a smoothed surface (monocrystalline layer 3) positioned between the strained channel layer 5 and the Si substrate 1; and a pMOSFET (p-channel transistor) and an nMOSFET (n-channel transistor), wherein the channel of the pMOSFET and the channel of the nMOSFET are formed in the strained channel layer 5. Evidence for the monocrystalline layer 3 being smoothed is disclosed by Lustig at column 4, lines 1-4 which states that the monocrystalline layer 3 should be reduced to a "desired thickness" by oxidation and etching. Thus, it must be inherent that such thickness is uniform throughout the entire monocrystalline layer 3. And since the thickness is the same throughout the entire layer, it must also be inherent that the top surface of the monocrystalline layer 3 is flat, smoothed or planar as a result of the reducing step.

Re claims 1 and 15, Lustig fails to show the following features: a SiGe graded buffer layer positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate., and the strained channel layer having an average roughness less than 1nm.

Chu et al. ("Chu") expressly teaches in Figure 1 to form a SiGe graded layer 13 positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer 14 and the Si substrate 12. However, Chu fails to disclose the strained channel layer having an average roughness less than 1nm.

Canaperi et al. ("Canaperi") suggests a planarized layer 74 having a surface roughness (RMS) of 0.5 to 0.8 nm which is acceptable or qualified for epitaxial growth of strained Si or SiGe (see col. 5, lines 35-58).

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Since Lustig, Chu and Canaperi are from the same field of endeavor, the purposes disclosed by Chu and Canaperi would have been recognized in the pertinent prior art of Lustig.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lustig with the suggestions of Chu and Canaperi because Chu states at column 1, lines 32-43 that such modification would provide a buffer layer with low dislocation densities, and Canaperi states at col. 5, lines 50-58 that such modification would prevent the continued roughening and grooving of the surface that leads to dislocation blocking and minimizes threading dislocation density during subsequent growth of the graded SiGe layer.

Re claims 4 and 18, Lustig expressly discloses in Figures 1-9 that the heterostructure further comprises an oxide layer 2 positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer 4 and the substrate 1.

Re claims 6 and 20, Lustig expressly discloses at column 3, line 60 that the strained surface layer 5 comprises silicon.

Re claims 12, 26 and 27, since the circuit as disclosed by Lustig comprises a CMOS inverter (see col. 2, lines 44-48), it should be inherent that the gate drive is reduced to lower power consumption, and the p-channel transistor serves as a pull-up transistor while the n-channel transistor serves as a pull-down transistor in the circuit.

Re claims 7-11 and 21, Lustig fails to show the specific parameters regarding the surface roughness of the strained layer, the Ge content "x" in the SiGe layer, or the ratio of gate width of the pMOSFET to the gate width of the nMOSFET.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Lustig by selecting the specific parameters as required by the

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claims, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

**Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lustig, Chu and Canaperi as applied to claims 1, 6-12, 15, 20, 21, 26 and 27 above, and further in view of Kant (U.S. 6,316,301).**

Re claims 22-25, the combined disclosure of Lustig, Chu and Canaperi fails to specify what types of devices could be formed using a CMOS circuit.

Kant teaches that CMOS circuits are used to form an inverter (see Fig. 1; col. 1, lines 37-40) and a number of suitable logic gates such as NOR gates, XOR gates and NAND gates (see Fig. 4; col. 4, lines 20-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the CMOS circuit of Lustig, in view of Canaperi et al., to form the devices as suggested by Kant because of the desirability to perform a variety of functions. Furthermore, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

#### ***Response to Arguments***

Applicant's arguments filed April 7, 2004 have been fully considered but they are not persuasive.

Applicant argues that both Lustig and Canaperi fail to disclose "a graded SiGe layer beneath a strained channel layer". The Examiner respectfully agrees but reminds Applicant that

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Chu cures such deficiencies of Lustig and Canaperi by expressly teaches in Figure 1 a SiGe graded layer 13 being positioned below a strained channel layer 16.

Applicant further argues that Chu fails to suggest "smoothing". Once again, the Examiner respectfully agrees but reminds Applicant that Lustig clearly discloses at column 4, lines 1-4 that the monocrystalline layer 3 should be reduced to a "desired thickness" by oxidation and etching. In order to have such a "desired thickness", the thickness of the monocrystalline layer 3 should be uniform throughout. And since the thickness is uniform throughout, it must be inherent that the top surface of the monocrystalline layer 3 is smoothed.

Furthermore, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, Chu and Canaperi cure the deficiencies of Lustig as follows:

a SiGe graded buffer layer positioned between the relaxed  $\text{Si}_{1-x}\text{Ge}_x$  layer and the Si substrate., and the strained channel layer having an average roughness less than 1 nm.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Thursday (9:00 AM - 6:00 PM).

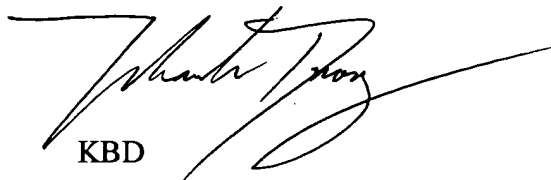
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR



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